Enhancing High-Quality Human Resource Training for Vietnam's Semiconductor Industry: A Policy-Systems Diagnosis and Strategic Solution Framework

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ABSTRACT:

Vietnam has committed to training at least 50,000 university-educated semiconductor professionals by 2030 under Decision No. 1017/QD-TTg, one of the most ambitious sectoral workforce targets announced by any middle-income economy. Yet as of late 2025 the country's semiconductor workforce stood at approximately 15,000 people, and fewer than 7,000 students were enrolled in dedicated semiconductor programmes. This paper asks why the gap between policy ambition and delivery capacity has proved so persistent, and what configuration of interventions would close it. Using a qualitative policy-systems design that triangulates primary legal instruments, ministerial implementation reports, industry workforce statistics and international benchmarking, the study develops a five-domain diagnostic framework demand articulation, supply throughput, pedagogical quality, enabling capacity (faculty and laboratories), and governance-finance and applies it to Vietnam's semiconductor human resource development system over the period 2023–2026. The analysis identifies five interlocking bottlenecks: a demand signal that is aggregated rather than segmented by value-chain stage; a supply pipeline whose apparent scale masks a narrow specialist core; a faculty base that is the binding constraint on expansion; a laboratory infrastructure programme immobilised by disbursement friction rather than by budget scarcity; and a governance architecture rich in strategy but thin in outcome measurement. A transparent throughput model demonstrates that the 2030 target is arithmetically attainable only under a hybrid pathway in which conversion and upskilling of adjacent-discipline engineers supplies the majority of near-term output while degree programmes scale behind it. The paper proposes an integrated five-pillar solution framework segmented capacity planning, a faculty capability surge, a shared-infrastructure utility, deep work-integrated learning, and outcome-based governance sequenced across three implementation horizons and stress-tested against four risk scenarios. The contribution is threefold: it supplies a replicable diagnostic instrument for sectoral workforce policy in latecomer economies; it reframes semiconductor talent formation as

a capacity-constrained throughput problem rather than an enrolment problem; and it offers Vietnamese policymakers a costed, sequenced and measurable reform agenda.

Keywords: semiconductor industry; high-quality human resources; higher education policy; workforce development; Vietnam; triple helix; technological catch-up

1. Introduction

The semiconductor industry occupies a structural position in the twenty-first-century economy comparable to that once held by steel or petroleum: it is simultaneously an industry, an input to nearly every other industry, and an instrument of geopolitical leverage. Global sales reached USD 627.6 billion in 2024, a 19.1 per cent year-on-year increase driven by artificial intelligence, and the sector is widely projected to approach one trillion dollars by 2030 (SEMI, 2025; Deloitte, 2023). Yet the binding constraint on that expansion is not capital and not fabrication capacity. It is people. Deloitte (2023) estimates that the industry, which employed slightly more than two million people directly in 2021, will need over one million additional skilled workers by 2030 more than 100,000 every year at a time when the graduate pipelines in the established producing economies are demonstrably too narrow to supply them. SEMI (2025) disaggregates this shortfall into more than 100,000 engineers in Europe and more than 200,000 in Asia-Pacific, and notes that the expansion also requires roughly 100,000 second-line and 10,000 third-line leaders, many of whom must be drawn from outside the industry altogether.

This global scarcity creates an unusual strategic opening for economies with young, mathematically capable populations and credible manufacturing track records. Vietnam is the most conspicuous such case in Southeast Asia. Having entered the global semiconductor value chain through the low value-added assembly, testing and packaging (ATP) segment anchored by Intel Products Vietnam in Ho Chi Minh City, Amkor Technology's plant in Bac Ninh, Hana Micron in the northern industrial belt and Samsung's module operations the country is projected to lift its share of global ATP capacity from approximately 1 per cent in 2022 to 8–9 per cent by 2032 (Semiconductor Industry Association & Boston Consulting Group, 2024). The Vietnamese state has since resolved to convert this position into something more durable. On 21 September 2024 the Prime Minister signed two mutually reinforcing instruments: Decision No. 1018/QD-TTg, which establishes the Strategy for Development of Vietnam's Semiconductor Industry to 2030 with a vision to 2050 under the formula C = SET + 1, and Decision No. 1017/QD-TTg, which approves the Programme on Development of Human Resources for the Semiconductor Industry to 2030 with orientations to 2050. Within that formula, the letter "T" talent is not one component among four but the precondition for the other three.

Decision 1017 is specific in a way that few workforce strategies are. By 2030 Vietnam is to train at least 50,000 people holding university degrees or higher for the semiconductor industry, of whom at least 42,000 at engineer and bachelor level, at least 7,500 at master's level and 500 at doctoral level; at least 15,000 are to serve the design stage and at least 35,000 the fabrication, packaging, testing and adjacent stages; at least 5,000 are to hold deep expertise in artificial intelligence applied to semiconductors; approximately 1,300 lecturers are to receive intensive specialist training; and four national-level shared laboratories together with eighteen institution-level standard laboratories are to be established, upgraded and modernised. These are testable commitments with a fixed horizon.

The counterfactual is equally specific. As of December 2025, Vietnam's semiconductor workforce comprised roughly 7,000 integrated-circuit design engineers, a further 7,000–8,000 engineers in packaging, testing, materials and equipment, and approximately 10,000 technicians — a total of about 15,000 people, supplemented by a network of more than 100 Vietnamese experts working abroad. On the training side, some 6,300 undergraduates were enrolled in semiconductor programmes, alongside around 600 master's students and 120 doctoral candidates, with just over 320 lecturers having completed specialist training

and ten small-scale laboratories constructed for practical instruction. The distance between 15,000 employed professionals and 50,000 trained graduates, to be traversed in under five years while the underlying teaching capacity is itself still being built, defines the policy problem this paper addresses.

That problem is not merely one of scale. Three features make it analytically distinctive. First, semiconductor competence is unusually tacit and equipment-embedded: a graduate cannot acquire it from lectures and simulation alone, because the discriminating skills — process integration, yield diagnosis, physical verification, failure analysis — are learned on instruments that cost more than a university department's annual budget. Second, the competence set is stage-specific and non-fungible: an engineer trained for register-transfer-level design is not deployable in a packaging line, and the 15,000/35,000 split written into Decision 1017 reflects a labour market with at least two largely separate skill economies. Third, the sector is subject to acute international poaching: any economy that succeeds in producing world-standard semiconductor engineers immediately becomes a supplier to the very shortage markets described above, so retention is a constitutive part of the training problem rather than an afterthought.

Vietnam's response since 2024 has been institutionally dense. Politburo Resolution No. 57-NQ/TW of 22 December 2024 elevated science, technology, innovation and digital transformation to the status of a national breakthrough, and was operationalised by Government Resolution No. 71/NQ-CP of 1 April 2025. Politburo Resolution No. 59-NQ/TW of 24 January 2025 reframed international integration as a strategic driver, and Politburo Resolution No. 71-NQ/TW of 22 August 2025 did the same for education and training. Directive No. 43/CT-TTg of 4 December 2024 targeted semiconductor and core digital technology training specifically. Decision No. 1131/QD-TTg of 12 June 2025 designated eleven strategic technologies and thirty-five strategic technology products, with semiconductors among them. The Law on Digital Technology Industry (Law No. 71/2025/QH15), adopted on 14 June 2025 and fully effective from 1 January 2026, created the first standalone statutory framework in the world dedicated to the digital technology industry, including targeted support for semiconductor human resource development. The Ministry of Education and Training issued a binding Training Programme Standard for semiconductor microelectronics at bachelor's and master's level (Decision No. 1314/QD-BGDDT of 13 May 2025, amended by Decision No. 2101/QD-BGDDT of 22 July 2025). Most recently, Decree No. 179/2026/ND-CP, effective 15 July 2026, introduced direct monthly scholarships for students in basic sciences, key engineering disciplines and strategic technologies.

Institutional density, however, is not the same as delivery. At the first 2026 meeting of the National Steering Committee on Semiconductor Industry Development, the Deputy Minister of Education and Training identified the shortage of research facilities and laboratories as an acutely pressing difficulty, noting that although a laboratory investment programme covering thirty universities exists, disbursement and project implementation remain stalled and unresolved. The same review recorded that ten of thirty-eight projects under the semiconductor strategy had been completed on schedule and twenty-four were on track, and that twenty-five localities had issued their own action plans — a picture of a system that is moving, but not yet at the velocity its own targets require.

Against this background, the paper addresses three research questions:

- **RQ1.** What is the actual state of Vietnam's semiconductor human resource development system in 2026, measured against the commitments in Decision 1017 and the requirements of the labour market it serves?
- **RQ2.** Which structural bottlenecks — as distinct from symptoms — account for the gap between policy ambition and delivery capacity?
- **RQ3.** What configuration and sequence of interventions would credibly close that gap, and under what conditions would it fail?

The paper makes three contributions. Theoretically, it integrates human capital theory, absorptive capacity and the triple helix into a five-domain diagnostic framework calibrated to sectoral workforce policy in latecomer economies, and argues that semiconductor talent formation is best understood not as an enrolment problem but as a throughput problem governed by capacity constraints upstream of the student. Empirically, it assembles and reconciles the dispersed 2024–2026 evidence base on Vietnamese semiconductor training — legal instruments, ministerial implementation

reporting, industry workforce statistics and institutional disclosures — into a single verifiable account, and subjects the 2030 target to a transparent feasibility model. Practically, it proposes a five-pillar solution framework with explicit sequencing, institutional ownership, indicator sets and risk analysis, designed to be actionable by the Ministry of Education and Training, the Ministry of Science and Technology, provincial authorities and higher education institutions.

The remainder of the paper is organised as follows. Section 2 develops the theoretical framework and reviews the relevant literature. Section 3 sets out the research design. Section 4 presents the diagnostic findings across the five domains and models the feasibility of the 2030 target. Section 5 benchmarks Vietnam against four comparator systems and synthesises the structural bottlenecks. Section 6 develops the solution framework, implementation roadmap and risk analysis. Section 7 concludes.

2. Theoretical framework and literature review

2.1 Human capital, specificity and the limits of the enrolment metaphor

The foundational proposition that expenditure on education and training constitutes investment in a productive asset rather than consumption originates with Becker (1964), whose central analytical move the distinction between general and firm-specific human capital remains the most useful entry point into semiconductor workforce policy. Becker's insight was that the party who bears the cost of training is determined by the appropriability of its returns: general skills, being portable, are financed by the worker, while specific skills, being non-portable, are financed by the firm.

Semiconductor competence sits awkwardly across this dichotomy, and the awkwardness is policy-relevant. Much of it is *industry-specific* rather than either general or firm-specific: knowledge of process design kits, tape-out discipline, cleanroom protocol or automated test equipment is portable across employers within the sector but nearly worthless outside it. Industry-specific human capital is systematically under-supplied by both parties in Becker's framework — the worker will not finance it because the labour market for it is thin and risky at the point of decision, and the individual firm will not fully finance it because a trained engineer can be poached by a competitor the following quarter. This under-provision is the classical justification for public co-investment of precisely the kind Decision 1017 represents, and it explains why every major semiconductor economy has intervened rather than relying on market signals.

It also exposes the weakness of the enrolment metaphor that dominates public discussion of workforce targets. Counting students admitted to relevant programmes measures the *front* of the pipeline; what the industry consumes is the *exit* of the pipeline, filtered by attrition, by specialisation choice, by the quality of practical exposure, and by whether the graduate can be productive without a further six to twelve months of employer-funded remediation. A workforce target expressed in graduates trained is therefore not a target at all unless it is accompanied by conditions on the throughput and the quality of what emerges.

2.2 Absorptive capacity and the recursive problem of trainer supply

Cohen and Levinthal (1990) demonstrated that an organisation's ability to recognise, assimilate and apply new external knowledge is a function of its prior related knowledge, and that this absorptive capacity is cumulative and path-dependent: the ability to learn in period t depends on what was learned in period $t-1$.

Applied at the level of a national training system, absorptive capacity yields the single most important structural insight for this paper. A university cannot teach advanced semiconductor engineering unless it already possesses faculty who understand advanced semiconductor engineering; those faculty can only be produced by other institutions that already possess such faculty, or imported from industry and abroad. The system therefore exhibits a recursive bottleneck: the rate at which student capacity can expand is bounded above by the rate at which teaching capacity expands, and teaching capacity is the slower-moving variable by an order of magnitude. Decision 1017's provision for intensive training of approximately 1,300 lecturers is, on this reading, not a supporting measure but the load-bearing element of the entire programme.

The same logic applies to equipment. Absorptive capacity in a laboratory-dependent discipline is embodied not only in people but in instruments and in the institutional routines built around them. A laboratory delivered without trained operators, maintenance contracts and curricular integration adds far less

absorptive capacity than its capital cost suggests a consideration directly relevant to the assessment of Vietnam's stalled laboratory programme in Section 4.

2.3 National innovation systems and the triple helix

The national innovation systems tradition (Freeman, 1987; Lundvall, 1992; Nelson, 1993) established that innovative performance is a property of the interaction among firms, universities, research institutes and public agencies rather than of any single actor. Etzkowitz and Leydesdorff (2000) reformulated this as the triple helix, in which university, industry and government progressively assume one another's roles — universities becoming entrepreneurial, firms taking on educative functions, and the state acting as a venture organiser rather than a mere regulator — with innovation emerging from the overlay of communications among the three spheres. Etzkowitz, Webster, Gebhardt and Terra (2000) extended the argument to the internal transformation of the university itself.

For semiconductor workforce policy, the triple helix is analytically productive precisely because the three spheres possess complementary and non-substitutable assets. Industry holds the tacit process knowledge, the current tool-chains and the definitive statement of what competence means; universities hold the pedagogical infrastructure, the assessment machinery and the credentialing authority; government holds the fiscal capacity to overcome the under-provision problem identified in Section 2.1 and the convening authority to overcome coordination failure. Any configuration that omits one of the three fails predictably: university-led training without industry produces theoretically strong, operationally unemployable graduates; industry-led training without universities produces narrow firm-specific skills with no credential portability; state-led provision without either produces facilities that are neither used nor updated.

The triple helix also supplies the correct diagnostic vocabulary for weak linkage. In Etzkowitz and Leydesdorff's (2000) terms, Vietnam's semiconductor training system is transitioning from an *étatiste* configuration in which the state directs universities and industry from above — toward a genuine trilateral overlay, and the frictions observed in implementation are characteristic of that transition rather than evidence of its failure.

2.4 Latecomer catch-up and the East Asian precedent

A substantial historical literature examines how East Asian economies acquired semiconductor capability from a standing start. Amsden (1989) and Kim (1997) documented South Korea's state-coordinated learning trajectory; Hobday (1995) analysed the progression from original equipment manufacturing to own-design and own-brand manufacture across the East Asian latecomers; Mathews and Cho (2000) provided the definitive comparative account of semiconductor industry creation in Korea, Taiwan and Singapore, emphasising deliberate mechanisms of technology leverage and diffusion rather than autonomous invention. Fuller (2016) subsequently examined why comparable state effort in China produced markedly different outcomes, and Miller (2022) situated the whole trajectory within the geopolitics of the contemporary chip race.

Three lessons recur across this literature and structure the comparative analysis in Section 5. First, intermediary institutions matter more than either universities or firms individually: Taiwan's Industrial Technology Research Institute and its Electronics Research and Service Organisation, established alongside Hsinchu Science Park in 1980, functioned as translation devices between public research and commercial capability, and as the training ground from which commercial champions later spun off (Mathews & Cho, 2000; Trinh, Nguyen & Le, 2024). Second, co-location compresses learning cycles: physical proximity of firms, universities and shared facilities lowers the transaction cost of the interactions on which tacit knowledge transfer depends. Third, dependence on foreign direct investment alone does not generate indigenous capability, because multinational firms rationally withhold the process innovation knowledge that constitutes their core advantage; capability must be constructed through parallel domestic research and training investment, a conclusion Vietnamese analysts have drawn explicitly from the Taiwanese case (Trinh et al., 2024).

2.5 Semiconductor workforce studies and the Vietnamese evidence base

A distinct applied literature has emerged since 2021 in response to the global talent shortage. The National Academies of Sciences, Engineering, and Medicine (2024) analysed United States workforce needs in terms

of two separable reform agendas — higher education for research and development personnel, and technical workforce education for fabrication staff a distinction that maps directly onto Decision 1017's 15,000/35,000 split. The Semiconductor Industry Association and Oxford Economics (2023) quantified the United States labour market gap and recommended expansion of certification boot camps, apprenticeships and technical college programmes located near new fabrication facilities. Deloitte (2023) framed the shortage as a structural rather than cyclical phenomenon. Varas, Varadarajan, Goodrich and Yinug (2021) established the supply-chain geography within which national workforce strategies must be positioned.

On Vietnam specifically, the peer-reviewed evidence base remains thin. Trinh, Nguyen and Le (2024) provide the most substantial published treatment, documenting the shortage through synthesis of secondary sources, drawing lessons from Taiwan's TSMC-centred trajectory, and identifying four constraints on Vietnamese capability building: attracting learners into the field, inadequacy of training programmes, absence of leading domain experts, and the lack of a shared integrated-circuit design laboratory system. Their diagnosis is valuable and is corroborated by the present study. It is, however, constructed largely from pre-2024 material and therefore predates the entire policy architecture examined here, does not model the feasibility of the numerical targets, and does not offer a sequenced implementation design.

2.6 Research gap and conceptual framework

Three gaps follow from the foregoing. First, the existing Vietnamese literature is *descriptive-diagnostic* and pre-dates the 2024–2026 policy architecture; no study assesses whether the instruments now in force are internally coherent or sufficient. Second, no published work subjects the 50,000 target to arithmetic feasibility analysis, with the consequence that debate proceeds without an agreed view of whether and under what pathway the target is attainable. Third, the international workforce literature is overwhelmingly concerned with advanced economies possessing mature university-industry ecosystems, and its recommendations do not transfer unmodified to a system in which the faculty base is itself the scarce resource.

This paper addresses those gaps through the framework set out in Table 1, which decomposes a sectoral human resource development system into five interdependent domains. The framework's organising claim is that these domains are sequentially binding: a deficiency in an upstream domain cannot be compensated by effort in a downstream one. Scholarships (Domain 5) cannot produce competent graduates if laboratories do not exist (Domain 4); laboratories cannot produce competence if no one can teach with them (Domain 4); and neither matters if the specialisation mix does not correspond to what employers actually hire (Domain 1).

Table 1. Five-domain diagnostic framework for sectoral human resource development

Domain	Core question	Principal indicators	Theoretical anchor
D1. Demand articulation	Is required competence specified with sufficient granularity to be trainable against?	Stage-segmented demand forecasts; occupational standards; employer participation in specification	Human capital specificity (Becker, 1964)
D2. Supply throughput	Does the pipeline deliver sufficient qualified exits, not merely entries?	Enrolment, attrition, completion, specialisation mix, time-to-productivity	Throughput logic (Section 2.1)
D3. Pedagogical quality	Does the curriculum build tacit, equipment-embedded competence?	Practicum share, tool access, project cycles, industry placement, assessment validity	Absorptive capacity (Cohen & Levinthal, 1990)
D4. Enabling capacity	Do faculty and laboratory capacity permit expansion at the required rate?	Qualified faculty stock and growth; laboratory availability and utilisation; recurrent funding	Recursive bottleneck (Section 2.2)
D5. Governance and finance	Are actors coordinated, funded and held to measurable outcomes?	Institutional clarity; disbursement rates; outcome indicators; employer co-investment	Triple helix (Etzkowitz & Leydesdorff, 2000)

Source: Authors' construction.

3. Research design and methodology

3.1 Design rationale

The study adopts a qualitative policy-systems design with embedded quantitative feasibility modelling. Three considerations motivate this choice over a survey-based alternative.

First, the unit of analysis is a national policy system, not an individual or a firm; the causal mechanisms of interest — coordination failure, disbursement friction, recursive capacity constraints — operate at institutional level and are not observable through respondent perception. Second, the object of study is unusually well documented in the public record: the governing instruments are published legal texts with specific numerical commitments, and implementation is reported through ministerial conferences and steering committee reviews, permitting direct comparison of commitment against delivery without intermediation. Third, and decisively, the policy architecture is very recent — the core instruments date from September 2024 and the most consequential of them took effect in 2025 and 2026 — so that primary survey data collected now would capture a system in transition rather than in operation, and would risk substituting perception for the documentary record.

The design accordingly follows the logic of theory-guided document analysis with source triangulation, in which the five-domain framework of Table 1 supplies the analytical categories and the empirical task is to populate them from the strongest available evidence and to identify the points at which commitment and delivery diverge.

3.2 Data sources and corpus

The corpus comprises four source classes, assembled for the period January 2023 to August 2026:

(a) Primary legal and policy instruments. Politburo Resolutions 57-NQ/TW (2024), 59-NQ/TW (2025) and 71-NQ/TW (2025); Government Resolution 71/NQ-CP (2025); Prime Ministerial Decisions 1017/QD-TTg (2024), 1018/QD-TTg (2024) and 1131/QD-TTg (2025); Directive 43/CT-TTg (2024); the Law on Digital Technology Industry (Law No. 71/2025/QH15); Ministry of Education and Training Decisions 1314/QD-BGDDT (2025) and 2101/QD-BGDDT (2025); and Government Decree 179/2026/ND-CP.

(b) Implementation and administrative reporting. Ministry of Education and Training review conference reporting on Strategy 1018 and Programme 1017 (December 2025); National Steering Committee on Semiconductor Industry Development proceedings (2026); Ministry of Science and Technology industry statistics; and institutional admissions and programme disclosures from higher education institutions offering semiconductor programmes.

(c) Industry and sectoral data. Workforce and enterprise statistics for the Vietnamese semiconductor sector; global workforce and market analyses from Deloitte (2023), SEMI (2025), the Semiconductor Industry Association and Oxford Economics (2023), and Varas et al. (2021); and disclosures relating to major domestic capacity investments including the Viettel fabrication plant and the FPT testing and packaging facility.

(d) Scholarly literature. The theoretical and applied works reviewed in Section 2, retrieved through targeted searching of the international literature on semiconductor workforce development, technological catch-up and university–industry linkage.

3.3 Analytical procedure

Analysis proceeded in four steps. In Step 1 (framework operationalisation), each of the five domains in Table 1 was specified as a set of observable indicators with an associated evidence requirement. In Step 2 (evidence mapping), the corpus was coded against those indicators, with each substantive claim traced to a source and, where possible, corroborated by a second independent source; discrepancies between sources were retained and reported rather than reconciled by selection. In Step 3 (gap identification), commitments extracted from the legal instruments were compared with reported delivery, and the resulting gaps were classified as *quantitative* (a shortfall in volume), *qualitative* (a shortfall in competence) or *structural* (an absent or non-functioning mechanism). In Step 4 (feasibility modelling), a transparent throughput model was constructed to test the arithmetic attainability of the 2030 target under alternative pathways, using only published parameters and explicitly stated assumptions.

The solution framework in Section 6 was then derived by mapping each identified structural bottleneck to an intervention class, sequencing the interventions according to the dependency logic embedded in the

framework, and stress-testing the resulting design against four adverse scenarios.

3.4 Validity, reliability and limitations

Construct validity is supported by anchoring each analytical domain in an established theoretical tradition and by specifying indicators before evidence collection. Reliability is supported by the exclusive use of publicly retrievable sources, so that the evidence chain can be independently reconstructed. Triangulation across source classes mitigates the risk of over-reliance on official self-reporting: where administrative reporting is optimistic, it is read against independent industry statistics and institutional disclosures.

Four limitations should be stated plainly. First, the study contains no primary survey or interview data; the perceptions of students, faculty and employers are represented only as they appear in the documentary record, and a subsequent mixed-methods study incorporating employer competence assessments and graduate destination tracking would materially strengthen the findings. Second, certain administrative statistics are reported inconsistently across official communications — for example, estimates of the semiconductor workforce in packaging and testing vary between approximately 6,000 and 7,000–8,000 depending on the reporting occasion and on whether technicians are included; where such variation exists, it is reported as a range rather than resolved arbitrarily. Third, the feasibility model in Section 4.7 is illustrative rather than predictive: it is constructed to expose the arithmetic implications of published parameters, and its outputs are sensitive to assumptions that are stated explicitly and should be re-estimated as better data become available. Fourth, the policy architecture is evolving rapidly, and instruments enacted after August 2026 are outside the analysis.

4. Findings: the state of Vietnam's semiconductor human resource system

4.1 Domain 1: Demand articulation

Vietnam's demand signal is unusual among middle-income economies in being both official and numerically specific. Decision 1017 does not merely assert a need for more engineers; it segments the requirement into design (at least 15,000) and fabrication, packaging, testing and adjacent stages (at least 35,000), differentiates by qualification level (42,000 bachelor and engineer, 7,500 master, 500 doctorate), and carves out a distinct cohort of at least 5,000 with deep artificial intelligence expertise serving the semiconductor industry. Decision 1131/QD-TTg subsequently embedded semiconductors within a designated list of eleven strategic technologies and thirty-five strategic technology products, providing a stable reference point for training, research and investment prioritisation.

The demand structure is, moreover, being anchored by verifiable industrial commitments rather than projection alone. On 16 January 2026 Viettel Group broke ground on Vietnam's first semiconductor fabrication plant, a 27-hectare facility in Hoa Lac Hi-Tech Park assigned by the Ministry of National Defence under a Government resolution, with construction and technology transfer targeted for completion by the end of 2027, trial production thereafter, and process optimisation through 2030; at full operation the plant is designed for 3,000–4,000 wafers per month, equivalent to the minimum scale of a complete fabrication line and approximately 100 million chips annually. Twelve days later, on 28 January 2026, FPT Corporation announced the establishment of the country's first wholly Vietnamese-owned semiconductor testing and packaging plant, with a first phase during 2026–2027 in Yen Phong II-C Industrial Park, Bac Ninh, comprising 1,600 square metres, six functional test lines and specialised reliability and durability testing systems. Vietnam thus acquires, for the first time, domestic demand for front-end process engineers a competence class for which no domestic employer previously existed. The surrounding industrial base is substantial and growing: sector revenue was projected to exceed USD 21 billion in 2025, with more than USD 14 billion of foreign investment committed across over 240 projects, and approximately 60 integrated-circuit design companies now operating in the country.

Two weaknesses nonetheless persist in this domain.

The first is granularity below the two-stage split. The 15,000/35,000 division is a value-chain segmentation, not an occupational one. Within the 35,000, the competence requirements of a process integration engineer in a wafer fabrication plant, an equipment maintenance technician on an automated test line, a materials engineer, and a reliability engineer are substantially disjoint; within the 15,000, digital front-end design, analog and mixed-signal design, physical design, and design verification constitute distinct labour markets with distinct scarcity profiles. Absent occupational

standards at this level, higher education institutions design programmes against an aggregate signal and converge on the segments that are cheapest to teach predominantly digital design, which requires software licences rather than cleanrooms.

The second is the absence of an institutionalised employer voice in specification. The Training Programme Standard was developed through consultative fora convened by the Ministry of Education and Training, and individual institutions have established bilateral relationships with employers — the collaboration between Thai Nguyen University of Information and Communication Technology and Samsung on workforce development for Samsung's semiconductor operations in Thai Nguyen is a well-documented example, as is the engagement of senior specialists from Sunny Opotech Vietnam with Thai Nguyen University of Sciences on production lines, cleanroom management and component packaging during December 2025 and May 2026. These are valuable but bilateral and episodic. There is no standing sectoral skills body with the authority and the periodicity to translate employer requirements into revisable occupational standards, which is the mechanism by which comparable economies keep curricula synchronised with a technology frontier that moves annually.

4.2 Domain 2 Supply throughput

The supply picture requires careful disaggregation, because the headline figures and the operative figures differ by more than an order of magnitude.

At the widest aperture, Vietnam possesses more than 240 universities, of which approximately 166 offer engineering programmes, collectively training on the order of 134,000 engineering students annually. The same figure of 166 institutions is separately reported as the number of higher education institutions offering semiconductor-related courses a coincidence that is itself diagnostic, indicating that "institutions with engineering provision" and "institutions with semiconductor provision" are not being distinguished in administrative reporting, and that the apparent breadth of semiconductor training capacity may be an artefact of definitional imprecision. In the 2025 admissions cycle, more than 237,000 students were admitted to STEM disciplines, of whom more than 137,000 entered fields described as related to microchips and semiconductors.

At the narrow aperture students actually enrolled in dedicated semiconductor programmes the figure as reported by the Ministry of Education and Training in December 2025 was approximately 6,300 undergraduates, together with around 600 master's students, 120 doctoral candidates and more than 1,600 graduates of short-term technical programmes. A further cohort exceeding 12,000 students in adjacent fields is expected to transition into the sector through supplementary conversion training.

The distance between 137,000 and 6,300 is the single most important number in this analysis, and it is easily misread in either direction. It does not mean that only 6,300 students are relevant: the electrical, electronics, materials, physics, computer engineering and automation cohorts are the reservoir from which semiconductor specialists are drawn, and conversion is a legitimate and internationally standard pathway. But neither does it mean that 137,000 constitutes a semiconductor pipeline: without conversion modules, tool access and industry placement, an electronics graduate is not a semiconductor engineer, and the fraction of students actually pursuing semiconductor specialisation remains low by international comparison.

Three further supply observations follow.

First, the growth increment is currently dominated by conversion, not by initial degrees. Across 2025 Vietnam increased its stock of semiconductor design engineers by close to 1,000, achieved principally by upskilling engineers already working in related fields. This is the correct near-term instrument — it produces productive engineers in months rather than years — but it draws on a finite reservoir of experienced adjacent-field engineers and cannot be the primary mechanism through 2030.

Second, institution-level enrolment volumes are small relative to the target. Programme quotas disclosed for the 2026 cycle illustrate the scale: Hanoi University of Industry planned 100 places in semiconductor microelectronics; the University of Science, Vietnam National University Hanoi, planned 980 places across the semiconductor-related cluster, of which 140 in semiconductor technology specifically within materials science; the University of Engineering and Technology at the same national university planned 480 places in electronic engineering technology. Thai Nguyen University of Information and Communication Technology, a mid-tier provincial institution, admitted

46 students against a quota of 30 in 2024–2025 and 50 against 50 in 2025–2026 — evidence that demand from applicants exists at this scale, but also that individual programmes operate in the tens rather than the hundreds.

Third, the aggregate STEM share of enrolment remains below what the strategy assumes. Students in STEM disciplines account for approximately 27–29 per cent of total university enrolment, against a government orientation of 35 per cent by 2030. The semiconductor target is therefore being pursued from within a STEM base that is itself the object of a separate expansion effort, and the two are in competition for the same secondary school cohort.

4.3 Domain 3 Pedagogical quality

Vietnam's most substantial and least appreciated achievement in this area is the issuance of a binding training programme standard. Decision No. 1314/QD-BGDDT of 13 May 2025 established minimum common requirements applicable to all bachelor's and master's programmes training personnel for the semiconductor industry, covering objectives, learning outcomes, admission standards, learning volume, structure, content, teaching and assessment methods, faculty requirements, and physical facilities, technology and learning materials. It functions both as a floor for programme design and as the basis for major–minor, double-degree and interdisciplinary configurations.

Three features of the standard are consequential for quality.

Practical exposure is mandated, not encouraged. Practicum, laboratory work and real-world experience must constitute at least 25 per cent of total credits in the professional education and graduation components for bachelor's and level-6 engineer programmes, rising to at least 30 per cent for level-7 engineer programmes. Research-oriented postgraduate programmes require 24–30 credits of research work, comprising 12–15 credits of thesis and 12–15 credits of projects and research topics; applied postgraduate programmes require 6–9 credits of internship and 6–9 credits of graduation work. Internships and practical components are to be conducted, wherever possible, at industrial facilities or at specialised semiconductor research laboratories, and graduation projects must address one of the principal stages of the semiconductor value chain. This directly targets the equipment-embedded, tacit competence problem identified in Section 2.2.

Quantitative foundations are protected. Mathematics, basic sciences and informatics must account for at least 30 credits, designed appropriately to each specialisation — a defence against the common failure mode in which a programme is rebranded for a strategic sector while its analytical core is diluted.

Admission is quality-gated, and the gate has been calibrated. The original standard required a minimum mathematics score, which proved misaligned with the distribution of national examination results. Decision No. 2101/QD-BGDDT of 22 July 2025 replaced the absolute threshold with a relative one: candidates admitted on the basis of the national upper-secondary graduation examination must present an admission combination including mathematics and at least one appropriate natural science subject, and must fall within the top 25 per cent nationally on the admission combination score and the top 20 per cent nationally on mathematics. Holders of an existing bachelor's degree require a cumulative grade point average of at least 2.8 on a 4.0 scale, and students transferring from other programmes at least 2.5. The shift from an absolute to a percentile criterion is technically superior — it is invariant to year-on-year variation in examination difficulty — and signals a policy preference for selectivity over volume.

The gap in this domain is not the standard but the conditions of its execution. A mandated 25–30 per cent practicum share is a quality instrument only where laboratories, licensed tool-chains and placement capacity exist to absorb it; where they do not, the requirement is met nominally through simulation exercises and observational site visits. The evidence reviewed in Section 4.4 indicates that these conditions are not yet uniformly present, which converts an excellent standard into a source of compliance risk. Institutions that have invested seriously — the establishment of a specialised microchip laboratory at Thai Nguyen University of Sciences in consultation with Korean engineering experts, with modules in cleanroom technology, thin-film technology and microelectronic packaging, is an instructive case — demonstrate what compliance looks like when resourced.

4.4 Domain 4 Enabling capacity: faculty and laboratories

This is the domain in which the gap between commitment and delivery is widest, and, by the recursive logic of Section 2.2, the domain that governs the feasibility of everything else.

Faculty. Decision 1017 provides for intensive specialist training of approximately 1,300 lecturers. As reported by the Ministry of Education and Training in December 2025, more than 320 lecturers had received such training approximately a quarter of the target, at roughly the one-third point of the programme period. Ministry officials have concurrently identified a significant shortage of lecturers and scientists specialising in the field, attributed to the absence of adequate policies for attracting expertise. The mechanism of that shortage is structural rather than administrative: the alternative employment available to a semiconductor specialist, whether in a domestic design centre or abroad, is remunerated on a scale that public university salary schedules cannot approach, and the constraint therefore cannot be relieved by recruitment effort alone. Institutional responses exist several leading institutions have implemented talent attraction policies but they operate at the margin of a system-wide compensation structure.

Laboratories. Decision 1017 provides for four national-level shared semiconductor laboratories and eighteen institution-level standard laboratories. Reported delivery as of December 2025 comprised ten small-scale laboratories constructed for practical training. Proposals for the national shared laboratories are directed to Vietnam National University Ho Chi Minh City, Vietnam National University Hanoi, Da Nang and the National Innovation Centre, with the Ministry of Finance having consolidated budget proposals and deployment planned during 2026.

The most significant finding in this domain is that the binding constraint is disbursement, not appropriation. At the 2026 National Steering Committee review, the Deputy Minister of Education and Training identified the shortage of research facilities and laboratories as an extremely pressing difficulty and stated that although a laboratory investment programme covering thirty universities exists, its disbursement and project implementation remain stalled and unresolved. This is a materially different diagnosis from underfunding, and it implies a materially different remedy: procurement and public investment management reform rather than additional budget authority. Complementary measures have begun to address the equipment supply side Circular No. 30/2025 of the Ministry of Science and Technology permits enterprises to import used machinery and equipment for semiconductor production up to twenty years old, double the previous limit, and exempts educational and research institutions from age restrictions altogether — but permission to import is not the same as capacity to procure, install, staff and operate.

Shared infrastructure. A partial substitute has recently emerged. In mid-2026 the Ministry of Science and Technology launched a National Centre for Semiconductor Chip Prototyping Support, providing design tools, supporting design validation and verification, and acting as an intermediary with foundries, packaging and testing units and international technology partners to organise pilot production for universities, research institutes and domestic enterprises, with subsequent support for chip quality assessment and commercialisation; a post-silicon evaluation, testing and analysis laboratory is planned. In the 2026–2027 phase the State will fund 100 per cent of pilot production costs. This is precisely the intermediary institution the East Asian literature identifies as decisive (Section 2.4), and its design shared access to capability no single university can afford is the correct structural response to the laboratory constraint.

4.5 Domain 5: Governance and finance

Governance. The institutional architecture is now dense and reasonably clear. A National Steering Committee on Semiconductor Industry Development operates at Deputy Prime Ministerial level. The Ministry of Education and Training issued Plan No. 1758 in November 2024 to operationalise Decisions 1017 and 1018, and advised the Prime Minister to issue Directive No. 43 in December 2024. Twenty-five localities have issued their own action plans. Of thirty-eight projects under the strategy, ten were completed on schedule and twenty-four were on track at the time of the 2026 review, with none reported behind schedule.

Coordination among training institutions has also deepened. The five-university coalition initiated by the Ministry of Education and Training in Da Nang in 2023 — comprising Hanoi University of Science and Technology, Vietnam National University Ho Chi Minh

City, Vietnam National University Hanoi, the University of Da Nang and the Posts and Telecommunications Institute of Technology — was extended on 27 November 2025 when Vietnam National University Hanoi launched a semiconductor alliance linking education, research and industry with the objective of developing an open ecosystem and "Make in Vietnam" semiconductor products. Vietnam National University Hanoi has additionally invested in research infrastructure and is building a national centre for integrated-circuit design, manufacturing and testing.

The weakness is not coordination but measurement. Progress is reported predominantly in terms of activity and process — projects completed, plans issued, alliances launched, lecturers trained — rather than in terms of labour market outcomes. There is no published indicator set covering graduate placement into semiconductor employment, employer-assessed competence at hire, time-to-productivity, retention at twenty-four months, or the ratio of domestic hires to imported specialists in domestic firms. Without such indicators the system cannot distinguish between producing 50,000 graduates and producing 50,000 semiconductor professionals, and cannot detect quality failure until employers report it.

Finance. The most consequential recent instrument is Decree No. 179/2026/ND-CP, effective 15 July 2026, which introduces monthly scholarships for students in basic sciences, key engineering disciplines and strategic technologies, applying to cohorts admitted from 2025 onwards with disbursement beginning 1 September 2026. Undergraduate awards range from approximately VND 3.7 million to VND 5.5–5.6 million per month depending on discipline and programme type, with the higher rate applying to talent-track programmes and to semiconductor microelectronics. The design departs from precedent in directing support to the learner rather than through the institution: students apply to universities offering eligible programmes and, upon admission, receive the scholarship transferred via the institution. Approximately 22,250 students from the 2025 intake are expected to qualify, at a cost of some VND 350 billion; from the 2026 intake, support is anticipated for ten months per year at a total cost of approximately VND 4,200 billion per cohort.

Complementary fiscal support arrives through the Law on Digital Technology Industry, which extends special investment incentives to semiconductor design, production, packaging and testing projects, provides for local-budget support to semiconductor chip design enterprises covering human resource training and development, research and development, trial production and equipment procurement, and grants a five-year personal income tax exemption to high-quality personnel working in concentrated digital technology zones. The financing architecture thus addresses learner incentives, enterprise co-investment and specialist retention simultaneously — a more complete design than most comparable programmes achieve.

4.6 Synthesis of the diagnostic

Table 2 consolidates the findings by domain, classifying each gap by type.

Table 2. Commitment, delivery and gap classification by domain

Domain	Principal commitment	Reported delivery	Gap type	Severity
D1. Demand articulation	15,000 design / 35,000 fabrication-ATP split; 5,000 AI specialists; strategic technology designation	Split established; anchor demand created by Viettel fab and FPT ATP plant	Structural: no occupational standards below stage level; no standing sectoral skills body	Moderate
D2. Supply throughput	≥50,000 by 2030 (42,000 bachelor/engineer; 7,500 master; 500 doctorate)	~6,300 undergraduates, ~600 master's, ~120 doctoral in dedicated programmes; >12,000 conversion candidates identified; ~1,000 design engineers added in 2025 via upskilling	Quantitative: dedicated enrolment an order of magnitude below trajectory	High

Domain	Principal commitment	Reported delivery	Gap type	Severity
D3. Pedagogical quality	Binding standard: ≥25–30% practicum; ≥30 credits mathematics and basic sciences; percentile-based admission gate	Standard issued and amended; adoption uneven; execution conditional on facilities	Qualitative: compliance risk where laboratories and placements are unavailable	High
D4. Enabling capacity	~1,300 lecturers intensively trained; 4 national + 18 institutional laboratories	>320 lecturers trained; 10 small laboratories; 30-university laboratory programme stalled at disbursement; national prototyping centre launched 2026	Structural: recursive faculty constraint; public investment execution failure	Critical
D5. Governance and finance	Steering committee; ministerial plans; scholarship and tax instruments	10/38 projects complete, 24 on track; 25 local action plans; Decree 179 scholarships from 09/2026; DTI Law incentives	Structural: activity-based rather than outcome-based measurement	Moderate

Source: Authors' analysis of the sources described in Section 3.2.

4.7 Feasibility of the 2030 target: a transparent throughput model

Debate about the 50,000 target has proceeded largely without an agreed arithmetic. This section supplies one. The model is deliberately simple and its parameters are drawn from published figures; it is offered as an instrument for reasoning about pathways, not as a forecast.

Definitions and assumptions. Let T = 50,000 be the cumulative target of university-level or higher personnel trained for the semiconductor industry by 2030. Let the delivery window run from 2026 to 2030 inclusive (five years), since 2024 and 2025 were substantially occupied by architecture-building. Output is decomposed into three pathways:

- D — dedicated degree graduates: students enrolled in semiconductor-designated programmes who complete and enter the sector.
- C — conversion graduates: students in adjacent disciplines (electronics, electrical engineering, materials, physics, computer engineering, automation) who complete supplementary semiconductor modules and enter the sector.
- U — upskilled incumbents: working engineers from adjacent industries retrained through short intensive programmes at postgraduate or professional-certificate level.

Then $T = D + C + U$.

Pathway D. With approximately 6,300 undergraduates currently enrolled across a four-year cycle, steady-state annual output is of the order of 1,500 graduates before attrition. Applying a 15 per cent combined attrition and non-entry rate yields approximately 1,275 sector entrants per year at current enrolment. If dedicated enrolment grows at 30 per cent annually from 2026 — the upper end of the growth rate anticipated by the sector, and achievable only if Domain 4 constraints are relieved — first-year intakes rise from roughly 1,600 in 2026 to roughly 4,600 in 2030, but because of the four-year lag only the 2026 and 2027 intakes graduate within the window. Cumulative pathway D output for 2026–2030 is therefore of the order of 8,000–11,000, comprising the graduation of cohorts already in the system plus the earliest expanded intakes. Postgraduate output adds modestly: the current stock of approximately 600 master's and 120 doctoral candidates, expanding, contributes perhaps 3,000–4,000 master's and a few hundred doctoral completions across the window — well short of the 7,500 and 500 sub-targets unless postgraduate enrolment expands considerably faster than the undergraduate base.

Pathway C. The more than 12,000 students in related fields already identified as conversion candidates constitute the largest single reservoir. If conversion modules are made available at scale and two-thirds of identified candidates complete and enter the sector, pathway C contributes approximately 8,000; if the programme is extended to a larger share of the 137,000

students admitted to semiconductor-related fields in 2025 alone, and a conversion rate of 10 per cent is achieved across successive cohorts, pathway C could contribute 15,000–20,000 across the window. This is the most elastic pathway and the one most responsive to policy.

Pathway U. Vietnam added close to 1,000 design engineers in 2025 principally through upskilling. Sustaining that rate yields 5,000 across the window; tripling it through a national conversion academy model yields 15,000. The constraint here is the size of the pool of adjacent-industry engineers with sufficient prior related knowledge, and the willingness of employers to release staff for training.

Result. Under conservative assumptions (D = 11,000, C = 8,000, U = 5,000), cumulative output is approximately 24,000, or 48 per cent of the target. Under an aggressive but internally consistent set (D = 15,000, C = 20,000, U = 15,000), cumulative output reaches approximately 50,000. Three implications follow, and they are robust to reasonable variation in the parameters.

First, the target is not attainable through degree programmes alone, and no plausible expansion of undergraduate enrolment closes the gap within the window, because the four-year lag places most expanded intakes beyond 2030. Any strategy premised principally on opening new degree programmes will miss.

Second, conversion and upskilling must supply the majority of output to 2030, with dedicated degree programmes scaling behind them to serve the post-2030 steady state. This inverts the emphasis of much current institutional activity, which is concentrated on establishing new majors.

Third, the postgraduate sub-targets are the most at risk. The 7,500 master's and 500 doctoral commitments are disproportionate to current enrolment and depend most acutely on the faculty constraint, since doctoral supervision cannot be delivered by conversion training. If the faculty pipeline is not addressed as an immediate priority, the doctoral target will fail, and with it the system's capacity to reproduce itself after 2030.

5. Discussion: comparative benchmarking and structural bottlenecks

5.1 International benchmarking

Placing Vietnam alongside four comparator systems clarifies which of its difficulties are idiosyncratic and which are generic to semiconductor workforce building. Table 3 summarises the comparison.

Table 3. Comparative semiconductor workforce development approaches

System	Headline commitment	Distinctive mechanism	Transferable lesson for Vietnam
Taiwan (from 1980)	Industry creation rather than a numerical workforce target	Hsinchu Science Park co-located with two leading technical universities; ITRI and ERSO as public research and training intermediaries; deliberate spin-off of commercial champions; housing, schooling and healthcare provided to retain staff	Intermediary institutions and co-location, not enrolment expansion, are the primary instruments; retention is designed into the settlement, not left to salary
Republic of Korea	Reported ten-year roadmap to train 150,000 personnel; designated "semiconductor universities" within a national network, each hosting a semiconductor study centre	Regional distribution of specialised centres tied to a national network; deep state–chaebol coordination in curriculum and placement	A national network with regionally distributed specialised nodes avoids duplication while preserving geographic access
India (from 2022)	85,000 engineers in semiconductor design over ten years under Chips to Startup (C2S), within the	Free access to commercial EDA tools from Synopsys, Cadence, Siemens, Renesas, Ansys and AMD at 315 academic institutions, expanding to 500 under ISM 2.0; student designs fabricated and tested at the	Centralised tool licensing plus a national tape-out shuttle delivers hands-on capability at low marginal cost per institution — the

System	Headline commitment	Distinctive mechanism	Transferable lesson for Vietnam
	India Semiconductor Mission	Semiconductor Laboratory, Mohali, giving hands-on exposure across design, fabrication, packaging and testing; outlay of ₹250 crore over five years; predecessor SMDP-C2SD trained 52,365 personnel in its first five years	highest-leverage, lowest-cost intervention available to Vietnam
United States (from 2022)	Addressing a projected shortfall of approximately 67,000 unfilled roles by 2030	Two-track reform separating research and development workforce from technician workforce; certification boot camps, apprenticeships and community college programmes sited near new fabrication plants; industry co-funding matched by federal research agencies	Technician-level provision requires a distinct institutional track; siting training adjacent to plants materially improves placement

Sources: Trinh et al. (2024); Mathews and Cho (2000); Semiconductor Industry Association and Oxford Economics (2023); National Academies of Sciences, Engineering, and Medicine (2024); India Semiconductor Mission programme documentation.

Three comparative conclusions bear directly on the Vietnamese case.

The Indian C2S model is the most immediately transferable, because it addresses precisely the constraint that Vietnam has identified as most pressing. Rather than attempting to equip every institution, India centralised the procurement of commercial design tools and distributed access, then solved the tape-out problem — the step at which design education becomes real — through a national fabrication facility that manufactures and tests student designs. The marginal cost of adding an institution to such a scheme is small; the marginal cost of building it a laboratory is not. Vietnam's National Centre for Semiconductor Chip Prototyping Support, launched in 2026 with the State funding the full cost of pilot production during 2026–2027, is structurally the same instrument, and its scale-up is likely to yield a higher return per unit of expenditure than any other single measure available.

The Taiwanese lesson concerns institutional form rather than programme design. What distinguished Taiwan was not the volume of graduates but the existence of organisations — ITRI and ERSO — whose function was to hold capability that was too expensive for universities and too pre-commercial for firms, and to transfer it in both directions. Vietnam's National Innovation Centre and the new prototyping centre occupy this niche; the question is whether they will be resourced and staffed at the scale the role demands, or treated as coordinating secretariats.

The United States lesson concerns segmentation. The National Academies analysis (2024) treats semiconductor workforce reform as two distinct agendas because the institutions, credentials and pedagogies differ. Vietnam's 35,000-person fabrication, packaging and testing target will be filled predominantly by technicians and applied engineers, yet the policy conversation and the Training Programme Standard are framed around university degrees. The vocational and college sector is largely absent from the semiconductor workforce discussion, which is a strategic omission given that ATP operations are Vietnam's existing comparative advantage and its largest single employment requirement.

5.2 The five structural bottlenecks

Synthesising the domain findings against the comparative evidence yields five structural bottlenecks. They are stated as causal claims rather than as observations, and each is matched to a pillar of the solution framework in Section 6.

Bottleneck 1: Aggregate demand signalling produces adverse specialisation selection. Because demand is articulated at the level of two value-chain stages rather than at the level of occupations, and because no standing sectoral body converts employer requirements into revisable standards, institutions optimise against an ambiguous signal by selecting the specialisations with the lowest capital requirements. The predictable result is over-supply in digital design, where a software licence substitutes for a cleanroom, and under-supply in process integration, equipment engineering, packaging, testing,

reliability and materials — which is where 35,000 of the 50,000 required personnel are supposed to work, and where the Viettel and FPT investments will generate concrete demand from 2027.

Bottleneck 2 Pipeline architecture is mismatched to the delivery horizon. As Section 4.7 demonstrates, degree programmes cannot deliver the 2030 target because of the four-year lag, yet institutional and public attention is concentrated on opening new majors. The conversion and upskilling pathways, which are the only ones capable of delivering at the required rate within the window, are pursued opportunistically rather than as designed national programmes with dedicated funding, standardised curricula and recognised credentials.

Bottleneck 3 Faculty capacity is the binding constraint, and it is a compensation problem misdiagnosed as a recruitment problem. With approximately 320 of 1,300 target lecturers trained and an acknowledged shortage of specialist academics, the system's expansion rate is bounded by its teaching capacity. Because the opportunity cost facing a qualified semiconductor specialist is set by an international labour market in acute shortage, no volume of recruitment activity within existing public salary structures will resolve this. It is a structural pricing problem requiring structural instruments — differentiated remuneration, joint industry–university appointments, sabbatical exchange, and systematic mobilisation of the diaspora network of more than 100 overseas Vietnamese experts already convened under the National Innovation Network.

Bottleneck 4 Laboratory provision fails at execution, not at appropriation. The finding that a thirty-university laboratory investment programme is stalled at disbursement, reported at the highest level of the steering architecture, identifies public investment management as the operative constraint. Universities face procurement procedures designed for standard capital works, applied to specialised scientific instruments with long lead times, single-source suppliers, export-control considerations and substantial installation, calibration and maintenance requirements. Additional budget authority does not fix a procurement pathway that cannot execute the authority already granted.

Bottleneck 5 Governance measures activity rather than outcomes, so quality failure is invisible until employers detect it. Reporting in terms of projects completed, plans issued and lecturers trained cannot distinguish a graduate who is productive at hire from one requiring a year of remediation. Since the entire justification for the 50,000 target is the creation of employable capability, the absence of placement, competence-at-hire, time-to-productivity and retention indicators means the system's central claim is untested. This is also the domain in which the risk identified in Section 2.1 — international poaching of successfully trained engineers — would first become visible, and at present it would not be visible at all.

6. A five-pillar solution framework

The framework below maps one pillar to each bottleneck. Pillars are presented with their operative mechanisms, institutional ownership, and the indicators by which each should be judged. Section 6.6 sequences them; Section 6.7 stress-tests them.

6.1 Pillar 1 — Segmented demand articulation and occupational standards

Objective. Replace an aggregate demand signal with a granular, revisable and employer-validated specification of required competence, so that institutional supply decisions respond to actual scarcity.

Mechanisms.

1. Establish a Semiconductor Sector Skills Council as a standing tripartite body under the National Steering Committee, comprising the Ministry of Education and Training, the Ministry of Science and Technology, employer representatives spanning design houses, ATP operators, equipment and materials suppliers and the new domestic fabrication and packaging investments, and the leading training institutions. Its statutory function is to publish and biennially revise occupational standards.
2. Publish occupational standards for at least twelve semiconductor occupations, disaggregating the design segment into digital front-end design, analog and mixed-signal design, physical design and design verification, and the fabrication–ATP segment into process integration, equipment engineering, packaging engineering, test engineering, reliability engineering, failure analysis, materials engineering and cleanroom operations. Each standard specifies required competences, tool

proficiencies, assessment methods and the qualification levels at which the occupation is entered.

3. Publish a rolling three-year demand forecast by occupation and province, constructed from committed industrial investment rather than from aspiration, and updated annually. The Viettel fabrication plant's staffing schedule through trial production in 2027 and optimisation to 2030, and the FPT packaging and testing plant's phase-one requirements for 2026–2027, provide the initial anchor.

4. Condition programme approval and quota allocation on correspondence to the forecast, so that expansion in over-supplied specialisations is not funded at the same rate as expansion in scarce ones.

Ownership. Ministry of Education and Training and Ministry of Science and Technology jointly; council secretariat at the National Innovation Centre.

Indicators. Number of published occupational standards; proportion of accredited programmes mapped to them; forecast accuracy against realised hiring at twelve months; share of new programme approvals in scarce occupations.

6.2 Pillar 2 — A dual-track pipeline: conversion at scale now, degrees for the steady state

Objective. Align pipeline architecture with the delivery horizon by making conversion and upskilling the primary instruments to 2030 while degree capacity is built for the period beyond.

Mechanisms.

1. Establish a National Semiconductor Conversion Programme as a funded national programme rather than a set of institutional initiatives. It should offer standardised modular credentials of two to four semesters, stackable toward a master's qualification, targeted at the identified pool of more than 12,000 adjacent-discipline students and at final-year students within the much larger 137,000-strong semiconductor-related admissions cohort. Modules should be co-designed with employers against the Pillar 1 occupational standards and delivered jointly by consortium institutions to avoid duplication.

2. Create an Industry Upskilling Scheme for working engineers in adjacent industries, structured as intensive twelve- to twenty-four-week programmes with employer co-funding and a training levy offset. Vietnam's demonstrated capacity to add close to 1,000 design engineers in a single year through upskilling establishes the mechanism's viability; the task is to institutionalise and multiply it.

3. Open a technician and applied-engineer track through the vocational and college sector, aligned to the ATP occupational standards and sited adjacent to industrial zones in Bac Ninh, Thai Nguyen, Ho Chi Minh City, Da Nang and Hoa Lac. This addresses the largest single component of the 35,000 requirement and the component least well served by the current university-centric framing.

4. Protect the postgraduate pipeline by ring-fencing scholarship and research funding for master's and doctoral study in semiconductor fields, on the reasoning developed in Section 4.7 that the postgraduate sub-targets are the most at risk and that doctoral output is the mechanism by which the faculty constraint is ultimately relieved.

Ownership. Ministry of Education and Training, with the university alliances as delivery consortia and employers as co-funders.

Indicators. Conversion enrolments and completions; upskilling completions and employer co-funding ratio; technician-track enrolments; postgraduate enrolment growth; sector entry rate at six months post-completion by pathway.

6.3 Pillar 3 — A faculty capability surge

Objective. Relieve the recursive constraint by expanding qualified teaching capacity faster than student capacity, using instruments appropriate to a compensation problem rather than a recruitment problem.

Mechanisms.

1. Introduce a differentiated remuneration instrument for strategic technology faculty, structured as a fixed-term national supplement attached to the individual rather than the institution and conditional on teaching load and industrial currency. The personal income

tax exemption already available under the Law on Digital Technology Industry to high-quality personnel in concentrated digital technology zones establishes the precedent for differentiated treatment; extending an analogous instrument to strategic technology academics is a coherent continuation.

2. Institutionalise joint industry–university appointments, under which practising engineers from design houses, ATP operators and the new domestic plants hold formal fractional academic appointments with teaching and supervision obligations, and academics undertake structured industrial secondments. This simultaneously imports current tacit knowledge and reduces the salary gap by permitting dual income.

3. Convert the diaspora network into a teaching resource. The network of more than 100 Vietnamese semiconductor experts abroad convened under the National Innovation Network is presently an advisory asset. A structured visiting professorship scheme — intensive block teaching, doctoral co-supervision and curriculum review, delivered on short residencies compatible with continuing overseas employment — would convert advisory goodwill into instructional capacity at modest cost.

4. Accelerate the 1,300-lecturer training commitment through international partnership placements, prioritising the fabrication, packaging, testing and equipment specialisations that are currently under-supplied, and requiring each trained lecturer to deliver a defined quantum of onward training within the domestic system — a train-the-trainer multiplier that converts a linear commitment into a compounding one.

5. Fund doctoral supervision capacity explicitly, recognising that the 500-doctorate target is not achievable without a prior expansion in the number of academics qualified to supervise, and that this is the longest lead-time element of the entire programme.

Ownership. Ministry of Education and Training with Ministry of Home Affairs on remuneration instruments; institutions on appointments.

Indicators. Qualified specialist faculty headcount and growth rate; lecturers completing intensive training against the 1,300 target; joint appointments in force; diaspora teaching days delivered; doctoral supervision capacity; faculty attrition to industry and abroad.

6.4 Pillar 4 — A shared infrastructure utility and deep work-integrated learning

Objective. Make the mandated 25–30 per cent practicum requirement executable everywhere, by treating expensive capability as a shared utility rather than an institutional possession, and by embedding students in real production environments.

Mechanisms.

1. Scale the national prototyping centre into a full multi-project wafer shuttle service. The National Centre for Semiconductor Chip Prototyping Support already provides design tools, validation and verification support, and foundry, packaging and testing liaison for pilot production, with the State funding the full cost during 2026–2027. Establishing a predictable annual shuttle calendar — with guaranteed slots allocated to university design teams — would give every participating institution a route from design to fabricated, tested silicon, which is the single most effective means of converting theoretical instruction into demonstrable competence.

2. Centralise commercial tool licensing nationally, following the Indian precedent of negotiating EDA access with major vendors and distributing it to accredited institutions at zero or nominal marginal cost, delivered through cloud access to avoid per-site infrastructure requirements. This is the highest-leverage low-cost intervention identified in this study.

3. Resolve the laboratory disbursement blockage as a procurement reform, not a budget question. Specific measures: a specialised procurement pathway for scientific instrumentation permitting single-source justification and extended lead times; centralised procurement expertise available to

universities lacking it; mandatory inclusion of installation, calibration, maintenance and operator training in equipment packages; and public reporting of disbursement rates by institution to create accountability. The permission granted under Circular No. 30/2025 for educational and research institutions to import used equipment without age restriction should be paired with a curated register of qualified suppliers and refurbishment partners, so that the flexibility is usable in practice.

4. Mandate a substantive industrial placement in every semiconductor programme, of not less than one semester, with dual academic and industrial supervision, an assessed workplace project, and formal employer sign-off against the Pillar 1 occupational standards. The Training Programme Standard already encourages practical components at industrial facilities; converting encouragement into requirement, and requiring employer assessment, closes the loop between curriculum and competence.

5. Require a full design cycle in every design-track programme — specification, register-transfer-level design, verification, synthesis, physical implementation, sign-off and, wherever the shuttle permits, tape-out — rather than a sequence of disconnected laboratory exercises. Competence in this field is demonstrated by completed cycles, not by covered topics.

6. Co-locate training with production. Siting technician and applied-engineer provision adjacent to the Hoa Lac fabrication plant, the Bac Ninh packaging and testing cluster and the established ATP operations replicates the Hsinchu logic of compressing learning cycles through proximity, and materially improves placement rates.

Ownership. Ministry of Science and Technology and the National Innovation Centre on shared infrastructure; Ministry of Finance and Ministry of Education and Training on procurement reform; institutions and employers on placements.

Indicators. Institutions with EDA access; university tape-outs completed annually; laboratory disbursement rate; laboratory utilisation hours per student; students completing a semester-long assessed placement; employer sign-off pass rates.

6.5 Pillar 5 — Outcome-based governance, financing and retention

Objective. Shift measurement from activity to labour market outcomes, tie funding to those outcomes, and treat retention as a designed component of the training system.

Mechanisms.

1. Publish a national semiconductor workforce indicator set, reported annually, covering at minimum: enrolments and completions by pathway and occupation; graduate placement into semiconductor employment at six and twelve months; employer-assessed competence at hire; time-to-productivity; retention in the sector and in Vietnam at twenty-four and forty-eight months; faculty stock and growth; laboratory utilisation; and disbursement execution. Without these, the system cannot manage what it is attempting.

2. Make a share of institutional funding outcome-contingent, with an increasing proportion of programme funding released against verified placement and employer competence assessment rather than against enrolment. This directly counteracts the incentive to expand enrolment in cheap specialisations identified as Bottleneck 1.

3. Institutionalise employer co-investment through a training levy with offset against approved in-house and consortium training, converting the free-rider problem inherent in industry-specific human capital (Section 2.1) into a collective financing mechanism, and giving employers a direct financial stake in curriculum quality.

4. Design retention explicitly. The Taiwanese precedent locates retention in the totality of the settlement — housing, schooling, healthcare and quality of life around Hsinchu — rather than in salary alone. Vietnam's concentrated digital technology zones, with their five-year personal income tax exemption for high-quality personnel, provide the legal vehicle;

adding housing support, accelerated career structures and research funding access for returning specialists would complete it. Retention should be monitored as an indicator, not assumed.

5. Monitor the scholarship instrument for effect, not merely for disbursement. Decree No. 179/2026/ND-CP represents a substantial commitment — on the order of VND 4,200 billion per cohort from the 2026 intake — and is the first Vietnamese instrument to direct support to the learner rather than through the institution. Its evaluation should test whether it shifts the composition of applicants toward scarce specialisations and whether recipients enter and remain in the sector, not merely whether funds were transferred.

Ownership. National Steering Committee, with the Ministry of Education and Training as reporting authority and the Ministry of Finance on financing instruments.

Indicators. Publication and completeness of the indicator set; share of funding allocated on outcome criteria; levy participation and offset uptake; twenty-four-month sector retention and emigration rates; scholarship recipients entering the sector.

6.6 Implementation sequence

The pillars are not independent, and the order of implementation determines whether they compound or dissipate. Table 4 sets out a three-horizon sequence derived from the dependency logic of the diagnostic framework: enabling capacity and demand specification must precede volume expansion, because expanding volume against an unrelieved capacity constraint degrades quality rather than increasing output.

Table 4. Implementation sequence and priority

Horizon	Priority actions	Rationale	Lead
H1: 2026–2027 (unblock)	Resolve laboratory disbursement through procurement reform; negotiate national EDA licensing; scale the prototyping centre and establish a shuttle calendar; launch the faculty remuneration instrument and joint appointments; constitute the Sector Skills Council; publish the first occupational standards; launch the Conversion Programme and Upskilling Scheme	Relieves the binding constraint (Bottleneck 4) and the recursive constraint (Bottleneck 3) before volume expansion; activates the only pathways capable of delivering within the window (Bottleneck 2)	MOET, MOST, MOF, NIC
H2: 2028–2029 (scale)	Expand dedicated degree and technician-track enrolment against occupational forecasts; complete the 1,300-lecturer programme with train-the-trainer multipliers; bring national and institutional laboratories into full operation; mandate semester-long assessed placements; introduce outcome-contingent funding and the employer levy	Volume expansion now proceeds against relieved capacity; quality mechanisms bind as scale increases	MOET, institutions, employers
H3: 2030 and beyond (consolidate)	Shift the output mix from conversion toward dedicated degrees; expand doctoral output to reproduce faculty capacity; deepen specialisation in process, equipment, packaging and materials as domestic fabrication matures; institutionalise retention and diaspora return	Establishes a self-reproducing system rather than a one-off surge; aligns competence mix with an industry that by then possesses domestic front-end capability	National Steering Committee

Source: Authors' construction.

6.7 Risk analysis

Four scenarios would materially degrade the framework's outcomes. Each is stated with its leading indicator and its mitigation.

R1 Quality dilution under volume pressure. The most probable failure mode. Under pressure to demonstrate progress toward 50,000, institutions rebrand existing electronics programmes, satisfy the practicum requirement through simulation and site visits, and produce graduates who are semiconductor-qualified on paper and unemployable in practice. *Leading indicator:* rapid growth in enrolment unaccompanied by growth in laboratory utilisation or employer sign-off rates. *Mitigation:* outcome-contingent funding (Pillar 5), employer assessment against occupational standards (Pillars 1 and 4), and public reporting of placement outcomes by institution.

R2 Successful training, failed retention. Vietnam trains to international standard and the resulting engineers are recruited by the shortage markets of Taiwan, Korea, Japan, Europe and North America, converting a national investment into an export subsidy. This is not hypothetical: the global shortfall described in Section 1 guarantees demand. *Leading indicator:* rising twenty-four-month emigration among graduates of flagship programmes. *Mitigation:* explicit retention design (Pillar 5); acceptance that a managed level of circulation is beneficial provided return pathways exist, following the Taiwanese and Korean precedent of systematically recruiting back experienced diaspora.

R3 Demand deferral. The Viettel plant slips beyond its end-2027 technology transfer milestone, or the projected expansion of ATP investment moderates with the semiconductor cycle, leaving trained graduates without domestic employment and destroying the applicant confidence on which enrolment depends. *Leading indicator:* falling graduate placement rates alongside stable enrolment. *Mitigation:* forecast demand from committed investment only (Pillar 1); maintain the export-oriented option of supplying regional shortage markets under managed circulation; preserve pathway flexibility so that conversion capacity can be redirected.

R4 Institutional fragmentation. Provincial competition and institutional prestige-seeking produce many small, sub-scale programmes, each with insufficient faculty and equipment, rather than a smaller number of properly resourced centres. Twenty-five localities have issued action plans; the risk that each seeks its own laboratory is real. *Leading indicator:* proliferation of programmes with enrolments below viable scale and faculty-to-programme ratios falling. *Mitigation:* the shared utility model (Pillar 3 of the Korean comparison and Pillar 4 here), consortium delivery through the existing university alliances, and quota allocation conditioned on demonstrated capacity rather than on applications received.

7. Conclusion

Vietnam has committed to training at least 50,000 university-educated semiconductor professionals by 2030 from a base of approximately 15,000 employed practitioners and roughly 6,300 students in dedicated programmes. This paper has asked what stands between the commitment and its realisation, and what would move it.

The answer developed here is that Vietnam's difficulty is not a deficiency of strategy. Measured against comparable middle-income economies, the policy architecture assembled between September 2024 and July 2026 is unusually complete: a segmented numerical target with legal force, a binding training programme standard with a mandated practicum share and a percentile-based admission gate, a statutory framework for the digital technology industry, direct scholarships to learners, tax instruments for retention, a national steering apparatus, and a shared prototyping facility of exactly the intermediary type the East Asian precedent identifies as decisive. Few countries at Vietnam's income level have built as much as quickly.

The difficulty is one of delivery capacity, and it is concentrated in three places. First, the faculty base is the binding constraint on everything downstream, and because the alternative employment available to semiconductor specialists is priced by an international market in acute shortage, it is a compensation problem that recruitment effort alone cannot solve. Second, laboratory provision is failing at execution rather than at appropriation — a thirty-university investment programme stalled at disbursement is a public investment management problem, and additional budget authority will not fix a pathway that cannot execute the authority already granted. Third, the pipeline architecture is mismatched to the delivery horizon: the four-year lag in degree programmes means the 2030 target is arithmetically unattainable through new majors,

and can only be met if conversion and upskilling carry the majority of output while degree capacity is built for the period beyond.

From this diagnosis the paper has derived a five-pillar framework — segmented demand articulation and occupational standards; a dual-track pipeline privileging conversion and upskilling to 2030; a faculty capability surge using compensation, joint appointments and the diaspora; a shared infrastructure utility combining national tool licensing, a tape-out shuttle and procurement reform, coupled to mandatory assessed industrial placement; and outcome-based governance with designed retention. The pillars are sequenced across three horizons on the principle that capacity constraints must be relieved before volume is expanded, since expanding volume against an unrelieved constraint degrades quality rather than increasing output. Four risk scenarios have been specified with leading indicators and mitigations, of which quality dilution under volume pressure is the most probable and retention failure the most consequential.

Three implications generalise beyond Vietnam. First, sectoral workforce targets expressed as graduate counts are not operational targets unless accompanied by conditions on throughput and competence; the enrolment metaphor systematically misdirects attention to the front of a pipeline whose constraints lie elsewhere. Second, in technology fields where competence is equipment-embedded, shared national infrastructure dominates institutional provision on both cost and quality grounds, and the intermediary institution — ITRI in Taiwan, the Semiconductor Laboratory at Mohali in India, the prototyping centre in Vietnam — is the pivotal organisational form. Third, in any field subject to global talent scarcity, retention is a constitutive part of training policy rather than a subsequent concern, and a national system that does not measure emigration cannot know whether its investment has been realised or exported.

The study's principal limitation is its reliance on documentary and secondary evidence. Four extensions would materially advance the analysis: an employer competence assessment establishing where Vietnamese graduates actually stand against international hiring standards; a graduate destination and retention tracking study following cohorts at twelve, twenty-four and forty-eight months; a costed comparison of the marginal return to shared versus institutional laboratory investment; and a political economy analysis of the procurement blockage, which this paper identifies as a critical constraint but does not explain. Each would convert elements of the framework proposed here from reasoned design into tested policy.

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